ABSTRACT

A method for an image reducing processing circuit includes the memory architecture of two FIFO units. The method includes the following steps of: providing an input processing unit receiving

5   original image data and delivering the image data; providing a horizontal direction image processing unit receiving the image data from the input processing unit; providing a first step FIFO unit receiving the image data from the horizontal direction image processing unit to read and write the image data on the same access

10   frequency; providing a vertical direction image processing unit receiving the image data from the first step FIFO unit; providing a second step FIFO unit receiving the image data from the vertical direction image processing unit and implementing the readout/writing of the image data on two access frequency; and

15   providing an output processing unit receiving the image data from the second step FIFO unit and outputting reduced image.

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